PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/649,450	Confirmation No.: 5775
Applicant	: Michael Doogue, et al.	
Filed	: August 26, 2003	
T.C./A.U.	: 2831	
Examiner	: Hung V. Ngo	
Docket No.	: ALLEG-039PUS	
Customer No.	: 022494	

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to a Notification of Non-Compliant Appeal Brief dated June 29, 2009, please see remarks set forth below and attachments hereto.

REMARKS

Please find attached hereto, a replacement page 21 of 21 to replace page 21 of 21 of the Appeal Brief filed December 8, 2008 and also to replace an earlier replacement page for same filed on April 27, 2009. The attached replacement page indicates evidence relied upon during prosecution, indicates attachment of the evidence, and makes a statement indicating where in the record the evidence was previously entered by the Examiner.

Accordingly, the replacement page and the evidence are attached hereto as listed below. A particular paragraph recited in the above-identified Amendment is marked on page 4 of the evidence.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 500845.

Respectfully submitted,

Dated: July 17, 2009

DALY, CROWLEY, MOFFORD & DURKEE, LLP

By: [signature]

Kermit Robinson
Reg. No. 48,734
Attorney for Applicant(s)
354A Turnpike Street, Suite 301A
Canton, MA 02021-2714
Tel.: (781) 401-9988, Ext. 124
Fax: (781) 401-9966
kr@dc-m.com

Attachments:

1) Replacement page 21 of 21 to Appeal Brief filed December 8, 2008.
2) Wikipedia, "Semiconductor device fabrication,"
   http://en.wikipedia.org/wiki/Semiconductor_fabrication ,
   formerly at http://en.wikipedia.org/wiki/Fabrication_(semiconductor) .

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(ix) Evidence (attached)

The following evidence was referenced by URL on page 10 of an Amendment filed June 30, 2008, which Amendment was entered by the Examiner. The URL has since changed as indicated below. However, the subject matter appears to be unchanged since June 30, 2008.

Wikipedia, "Semiconductor device fabrication,"

http://en.wikipedia.org/wiki/Semiconductor_fabrication ,

formerly at http://en.wikipedia.org/wiki/Fabrication_(semiconductor) .

(x) Related Proceedings

None

Semiconductor device fabrication

From Wikipedia, the free encyclopedia

Semiconductor device fabrication is the process used to create chips, the integrated circuits that are present in everyday electrical and electronic devices. It is a multiple-step sequence of photographic and chemical processing steps during which electronic circuits are gradually created on a wafer made of pure semiconducting material. Silicon is the most commonly used semiconductor material today, along with various compound semiconductors.

NASA's Glenn Research Center cleanroom.

The entire manufacturing process from start to packaged chips ready for shipment takes six to eight weeks and is performed in highly specialized facilities referred to as fabs.

Contents

Wafers

A typical wafer is made out of extremely pure silicon that is grown into mono-crystalline cylindrical ingots (boules) up to 300 mm (slightly less than 12 inches) in diameter using the Czochralski process. These ingots are then sliced into wafers about 0.75 mm thick and polished to obtain a very regular and flat surface.

Once the wafers are prepared, many process steps are necessary to produce the desired semiconductor integrated circuit. In general, the steps can be grouped into two areas:[1]

- Front-end processing

- Back-end processing

Processing

In semiconductor device fabrication, the various processing steps fall into four general categories: deposition, removal, patterning, and modification of electrical properties.

- Deposition is any process that grows, coats, or otherwise transfers a material onto the wafer. Available technologies consist of physical vapor deposition (PVD), chemical vapor deposition (CVD), electrochemical deposition (ECD), molecular beam epitaxy (MBE) and more recently, atomic layer deposition (ALD) among others.
- Removal processes are any that remove material from the wafer either in bulk or selectively and consist primarily of etch processes, either wet etching or dry etching. Chemical-mechanical planarization (CMP) is also a removal process used between levels.
- Patterning covers the series of processes that shape or alter the existing shape of the deposited materials and is generally referred to as lithography. For example, in conventional lithography, the wafer is coated with a chemical called a “photoresist”. The photoresist is exposed by a “stepper”, a machine that focuses, aligns, and moves the mask, exposing select portions of the wafer to short wavelength light. The unexposed regions are washed away by a developer solution. After etching or other processing, the remaining photoresist is removed by plasma ashing.
- Modification of electrical properties has historically consisted of doping transistor sources and drains originally by diffusion furnaces and later by ion implantation. These doping processes are followed by furnace anneal or in advanced devices, by rapid thermal anneal (RTA) which serve to activate the implanted dopants. Modification of electrical properties now also extends to reduction of dielectric constant in low-k insulating materials via exposure to ultraviolet light in UV processing (UVP).

Many modern chips have eight or more levels produced in over 300 sequenced processing steps.

Front-end processing

"Front-end processing" refers to the formation of the transistors directly on the silicon. The raw wafer is engineered by the growth of an ultrapure, virtually defect-free silicon layer through epitaxy. In the most advanced logic devices, *prior* to the silicon epitaxy step, tricks are performed to improve the performance of the transistors to be built. One method involves introducing a "straining step" wherein a silicon variant such as "silicon-germanium" (SiGe) is deposited. Once the epitaxial silicon is deposited, the crystal lattice becomes stretched somewhat, resulting in improved electronic mobility. Another method, called "silicon on insulator" technology involves the insertion of an insulating layer between the raw silicon wafer and the thin layer of subsequent silicon epitaxy. This method results in the creation of transistors with reduced parasitic effects.

Silicon dioxide

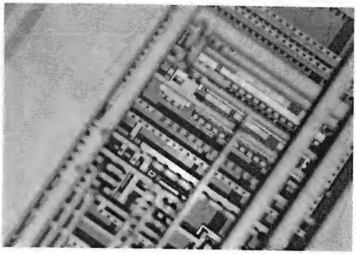
Front-end surface engineering is followed by: growth of the gate dielectric, traditionally silicon dioxide (SiO_2), patterning of the gate, patterning of the source and drain regions, and subsequent implantation or diffusion of dopants to obtain the desired complementary electrical properties. In memory devices, storage cells, conventionally capacitors, are also fabricated at this time, either into the silicon surface or stacked above the transistor.

Metal layers

Once the various semiconductor devices have been created they must be interconnected to form the desired electrical circuits. This "back end of line" (BEOL – the latter portion of the wafer fabrication, not to be confused with "back end" of chip fabrication which refers to the package and test stages) involves creating metal interconnecting wires that are isolated by insulating dielectrics. The insulating material was traditionally a form of SiO_2 or a silicate glass, but recently new low dielectric constant materials are being used. These dielectrics presently take the form of SiOC and have dielectric constants around 2.7 (compared to 3.9 for SiO_2), although materials with constants as low as 2.2 are being offered to chipmakers.

Interconnect

Historically, the metal wires consisted of aluminum. In this approach to wiring often called "subtractive aluminum", blanket films of aluminum are deposited first, patterned, and then etched, leaving isolated wires. Dielectric material is then deposited over the exposed wires. The various metal layers are interconnected by etching holes, called "vias," in the insulating material and depositing tungsten in them with a CVD technique. This approach is still used in the fabrication of many memory chips such as dynamic random access memory (DRAM) as the number of interconnect levels is small, currently no more than four.



Synthetic detail of a standard cell through four layers of planarized copper interconnect, down to the polysilicon (pink), wells (greyish) and substrate (green).

More recently, as the number of interconnect levels for logic has substantially increased due to the large number of transistors that are now interconnected in a modern microprocessor, the timing delay in the wiring has become significant prompting a change in wiring material from aluminum to copper and from the silicon dioxides to newer low-K material. This performance enhancement also comes at a *reduced cost* via damascene processing that eliminates processing steps. In damascene processing, in contrast to subtractive aluminum technology, the dielectric material is deposited first as a blanket film, and is patterned and etched leaving holes or trenches. In "single damascene" processing, copper is then deposited in the holes or trenches surrounded by a thin barrier film resulting in filled vias or wire "lines" respectively. In "dual damascene" technology, both the trench and via are fabricated before the deposition of copper resulting in formation of both the via and line simultaneously, further reducing the number of processing steps. The thin barrier film, called copper barrier seed (CBS), is necessary to prevent copper diffusion into the dielectric. The ideal barrier film is as thin as possible. As the presence of excessive barrier film competes with the available copper wire cross section, formation of the thinnest continuous barrier represents one of the greatest ongoing challenges in copper processing today.

As the number of interconnect levels increases, planarization of the previous layers is required to ensure a flat surface prior to subsequent lithography. Without it, the levels would become increasingly crooked and extend outside the depth of focus of available lithography, interfering with the ability to pattern.

CMP (chemical mechanical planarization) is the primary processing method to achieve such planarization although dry "etch back" is still sometimes employed if the number of interconnect levels is no more than three.

Wafer test

The highly serialized nature of wafer processing has increased the demand for metrology in between the various processing steps. Wafer test metrology equipment is used to verify that the wafers haven't been damaged by previous processing steps up until testing. If the number of dies—the integrated circuits that will eventually become chips— etched on a wafer exceeds a failure threshold (ie. too many failed dies on one wafer), the wafer is scrapped rather than investing in further processing.

Device test

Once the front-end process has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. The proportion of devices on the wafer found to perform properly is referred to as the yield.

The fab tests the chips on the wafer with an electronic tester that presses tiny probes against the chip. The machine marks each bad chip with a drop of dye. The fab charges for test time; the prices are on the order of cents per second. Chips are often designed with “testability features” such as "built-in self-test" to speed testing, and reduce test costs.

Good designs try to test and statistically manage *corners*: extremes of silicon behavior caused by operating temperature combined with the extremes of fab processing steps. Most designs cope with more than 64 corners.

Packaging

Once tested, the wafer is scored and then broken into individual die. Only the good, unmarked chips go on to be packaged.

Plastic or ceramic packaging involves mounting the die, connecting the die pads to the pins on the package, and sealing the die. Tiny wires are used to connect pads to the pins. In the old days, wires were attached by hand, but now purpose-built machines perform the task. Traditionally, the wires to the chips were gold, leading to a “lead frame” (pronounced “leed frame”) of copper, that had been plated with solder, a mixture of tin and lead. Lead is poisonous, so lead-free “lead frames” are now mandated by ROHS.

Chip-scale package (CSP) is another packaging technology. Plastic packaged chips are usually considerably larger than the actual die, whereas CSP chips are nearly the size of the die. CSP can be constructed for each die *before* the wafer is diced [1].

The packaged chips are retested to ensure that they were not damaged during packaging and that the die-to-pin interconnect operation was performed correctly. A laser etches the chip’s name and numbers on the package.

List of steps

This is a list of processing techniques that are employed numerous times in a modern electronic device and do not necessarily imply a specific order.

- Wafer processing
  - Wet cleans
  - Photolithography
  - Ion implantation (in which dopants are embedded in the wafer creating regions of increased (or decreased) conductivity)
  - Dry etching
  - Wet etching
  - Plasma ashing
  - Thermal treatments
    - Rapid thermal anneal
    - Furnace anneals
    - Thermal oxidation
  - Chemical vapor deposition (CVD)
  - Physical vapor deposition (PVD)
  - Molecular beam epitaxy (MBE)
  - Electrochemical Deposition (ECD). See Electroplating
  - Chemical-mechanical planarization (CMP)
  - Wafer testing (where the electrical performance is verified)
  - Wafer backgrinding (to reduce the thickness of the wafer so the resulting chip can be put into a thin device like a smartcard or PCMCIA card.)
- Die preparation
  - Wafer mounting
  - Die cutting
- IC packaging
  - Die attachment
  - IC Bonding
    - Wire bonding
    - Flip chip
    - Tab bonding
  - IC encapsulation
    - Baking
    - Plating
    - Lasermarking
    - Trim and form
- IC testing

Hazardous materials note

Many toxic materials are used in the fabrication process. These include:

- poisonous elemental dopants such as arsenic, antimony and phosphorus
- poisonous compounds like arsine, phosphine and silane
- highly reactive liquids, such as hydrogen peroxide, fuming nitric acid, sulfuric acid and hydrofluoric acid

It is vital that workers not be directly exposed to these dangerous substances. The high degree of automation common in the IC fabrication industry helps to reduce the risks of exposure of this sort. Most fabrication facilities employ exhaust management systems, such as wet scrubbers, combustors, heated absorber cartridges etc, to control the risk to workers and also the environment if these toxic materials are released into the atmosphere.

History

When feature widths were far greater than about 10 micrometres, purity was not the issue that it is today in device manufacturing. As devices became more integrated, cleanrooms became even cleaner. Today, the fabs are pressurized with filtered air to remove even the smallest particles, which could come to rest on the wafers and contribute to defects. The workers in a semiconductor fabrication facility are required to wear cleanroom suits to protect the devices from human contamination.

In an effort to increase profits, semiconductor device manufacturing has spread from Texas and California in the 1960s to the rest of the world, such as Europe, Israel, Japan, Taiwan, Korea, Singapore and China. It is a global business today.

The leading semiconductor manufacturers typically have facilities all over the world. Intel, the world's largest manufacturer, has facilities in Europe and Asia as well as the U.S. Other top manufacturers include STMicroelectronics (Europe), Analog Devices (US), Atmel (US/Europe), Freescale Semiconductor (US), Samsung (Korea), Texas Instruments (US), Advanced Micro Devices (AMD) (US/Germany) see [2], Toshiba (Japan), NEC Electronics (Japan), Infineon (Europe), Renesas (Japan), Taiwan Semiconductor Manufacturing Company (Taiwan, see TSMC web site), Chartered Semiconductor Manufacturing Ltd (Singapore, see Chartered web site), Sony(Japan), NXP Semiconductors (Europe), Micron Technology (US), Hynix (Korea) and SMIC (China, see SMIC web site).

See also

- Atomic layer deposition
- Cleanrooms
- Electronic design automation
- Foundry (electronics)
- GDS-II
- International Technology Roadmap for Semiconductors
- Microfabrication
- OASIS
- SEMI — The semiconductor industry trade association

References

1. ^ Zeno Gaburro (2004). "Optical Interconnect". in Lorenzo Pavesi and David J. Lockwood. *Silicon Photonics*. Springer. ISBN 3540210229. http://books.google.com/books?id=PgmmFRYE6a0C&pg=PA122&dq=%22front+end+process%22+transistor&lr=&as_brr=3&ei=elK_SKqAHZDwsgPRw63YDA&sig=ACfU3U3R53OZ9F-6x6e9woPK4C3fuxQJrw.

External links

- Amkor Technology Semiconductor Packaging & Test
- Semiconductor Manufacturing
- Semiconductor Glossary
- NEC's Virtual Factory Tour
- Semiconductor materials processing
- Calculator for Silicon thermal oxidation
- BYU Cleanroom - semiconductor properties, calculators, processes, etc.
- Omron An introduction to Application Expertise - Semiconductor, Photo Voltaic & Electronics Industry

Categories: Semiconductor device fabrication
Hidden categories: Articles needing additional references from September 2008 | Articles lacking in-text citations from September 2008 | Wikipedia external links cleanup